

Application No.: 09/811,435

Docket No.: 520.39869X00

REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This Amendment is in response to the Office Action dated December 4, 2003. Appreciation is expressed for the allowance of claims 6 and 7 and for the indication of allowable subject matter in claims 1-3 and 8-11.

By the present Amendment, each of the claims 1-5 and 8-12 has been amended in response to the 35 U.S.C. § 112, second paragraph, rejection in order to clarify the invention. Accordingly, reconsideration and removal of the 35 U.S.C. § 112, second paragraph, rejection is respectfully requested by virtue of these amendments.

With regard to the amendments, it is noted that the amendments to claim 1 have been made to define the invention based on the description set forth on page 13, line 10 et seq. concerning the feature of the invention that some bits are flipped according to pattern sequence number and the time in the pattern sequence. Other amendments have been made to adopt suggestions by the Examiner for eliminating or changing certain phraseology throughout the claims. By virtue of these amendments, each of the points raised on pages 2-5, line 2, of the Office Action have been addressed. Therefore reconsideration and removal of the 35 U.S.C. § 112, second paragraph, rejection is earnestly solicited.

Reconsideration and removal of the prior art rejections is also respectfully requested for the reasons set forth below. However, at the outset, it is noted that claim 5 has been amended to be a dependent claim, dependent on claim 1, which has already been indicated as containing allowable subject matter. More

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specifically, claim 5 has been amended to incorporate the language of claim 1 in its entirety. As such, since claim 1 has already been indicated as being allowable over the cited reference to Rajski (USP 6,327,687), reconsideration and removal of the rejection of claim 5 based on this reference is earnestly solicited.

In light of the above amendments and discussion, the sole remaining rejections in this case are the rejection of claim 12 under 35 U.S.C. § 102 as being anticipated by Spence (USP 5,258,985) and the rejection of claim 4 under 35 U.S.C. § 103 as being obvious over the Spence patent.

Reconsideration and removal of the 35 U.S.C. § 102 rejection of claim 12 as being anticipated by Spence is respectfully requested.

Claim 12 is directed to a feature of the invention of pattern generation in which the pattern has equal logical values set on adjacent FRS forming a part of a scan chain, shown, for example, in Fig. 31(c) and 31(d). Specifically, claim 12 defines generating test patterns by scan chain shift for a full scan design semiconductor integrated circuit wherein the scan chain shift is provided without any change in all scan chain inputs to set an identical logical value on neighboring storage elements on a scan chain. As such, pattern reducing variations of logic values are added to the scan chain. This has the effect of reducing the ratio of generation of transition signals during a scan chain shift or during a clock advancing time, thus reducing noise during the test.

It is respectfully submitted that the primary reference to Spence fails to teach or suggest the claimed method for generating such test patterns. On the contrary, Spence is directed to an arrangement for minimizing size of a BIST (Built-In Self Test) circuit by the combination of a data generator and a data analyzer. As

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discussed with regard to Fig. 3 of Spence, the method sets a state such as [000] in cells within a LFSR (Linear Feedback Shift Register), and adds them into the circuit under test. This serves to reduce the physical size of the BIST circuit to approximately half of a conventional circuit. Although this is of general interest, it does not teach or suggest the specific steps set forth in claim 12. Therefore, reconsideration and allowance of claim 12 over Spence is respectfully requested.

Reconsideration and allowance of claim 4 over Spence is also respectfully requested. Claim 4 is directed to the feature of providing a plurality of pattern generators (such as the pattern generator shown by numerals 921 and 922 in Fig. 17) which operate in two modes. In the first mode, each of the pattern generators generates a pattern independently. In the second mode, all of the pattern generators act as a shift register connected in series.

In Spence, on the other, there is no such teaching of a plurality of pattern generators capable of operating in the claimed two modes. As such, Spence lacks the advantage of the present invention that a plurality of pattern generators make it possible to reduce overhead preparing lines connecting scan chains in a circuit under test. Spence also lacks the advantage of the present invention that the claimed second mode provides a shift register, composed of the plurality of pattern generators, with the shift register having large bits to generate a pattern train which cannot be generated from a single pattern generator. Thus, it is possible to provide a very high fault coverage using a limited amount of test data. It is respectfully submitted that Spence completely lacks such features. Therefore, reconsideration and allowance of claim 4 over Spence is also respectfully requested.

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If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 520.39869X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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